Method and Interlevel Dielectric Structure for Improved Metal Step Coverage

U.S. Patent Application of:

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Background and Summary of the Invention

The present invention relates to integrated circuit structures and fabrication methods.

In integrated circuit fabrication, a key area of concentration has been the fabrication of contacts. Contact holes must usually be etched down through a significant thickness of interlevel dielectric, and significant issues arise. Contact holes are normally etched simultaneously to the active region and to the poly-1 level (polycide gate conductor), and thus the interlevel dielectric will be much thicker over some locations, especially when the dielectric has been planarized. (Planarization of the interlevel dielectric is highly desirable to minimize topographic excursion, but means that in some locations the contact holes may tend to have a very large aspect ratio.) This means that a large amount of overetch must be tolerated at the contacts to the poly-1 level.

For best mechanical properties of the metal layer, it would be desirable to provide sloped contact hole sidewalls. This has commonly been done with oxide reflow techniques, in which a short high-temperature treatment of a doped silicate glass produces nicely rounded corners (due to the surface tension effects on the silicate glass layer when it softens). One problem with this approach is that the required time at high-temperature is increasingly undesirable as geometries shrink.

Another approach has been to use a fairly isotropic etch, to produce a contact hole with sloped sidewalls; but this consumes a large area. The lateral spread of the contact sidewalls means that a significant spacing must be required between contacts to active and the

poly-1 layer, to prevent shorts to poly-1.

To achieve the best packing density, it would be desirable to use holes with nearly vertical sidewalls. However, such holes have a high aspect ratio (height/width ratio), and pose processing difficulties. Such geometries may present difficulties in completely filling the contact hole, or may cause an undesirable lack of planarity where the metal layer crosses over the hole. Such problems have been addressed by "stud contact" processes (where deposition and etchback of a highly conformal metal, such as W, precede deposition of a following metal such as Al:Cu). However, such processes add expense and complexity, and are more often used for vias than contacts.

One proposed method uses a second poly as the "landing pads" for bitline contacts in the matrix. In this way, the wordlines are protected thereby allowing for zero contact-to-gate spacing. The drawback is that this method cannot be used in the periphery due to contact resistance problems which result in slower operation of the device.

Another method uses a silicon nitride deposition on top of the polycide prior to pattern and etch. (*See* Singer, "A New Technology for Oxide Contact and Via Etch", SEMICONDUCTOR INTERNATIONAL, August 1993, p.36, which is hereby incorporated by reference.) Through the use of highly selective nitride to oxide etch selectivities, this will reduce the possibility of the contact touching the top of the polycide; however, it can still make contact along the sidewall due to the removal of the oxide spacer. Additionally, this does not address the problem of overetching the field oxide during the spacer etch.

Still another proposed method uses an Al_2O_3 etch-stop layer to

achieve a zero-margin contact process. (*See* Fukase *et al.*, "A Margin-Free Contact Process Using an Al_2O_3 Etch-Stop Layer for High-Density Devices," 1992 IEDM PROCEEDINGS 33.3, which is hereby incorporated by reference.)

The present application sets forth a new approach to contact formation, using a combination of isotropic and anisotropic etch steps to produce a contact profile which has steep sidewalls at its bottom portion and sloped sidewalls at its top portion. This approach recognizes that the constraints on the top part of the contact hole are different from those on the bottom part of the contact hole, and accordingly obtains the advantages of both steep-sidewall and sloped-sidewall geometries:

at the lower level, the contact occupies only a small area, and hence it is not necessary to impose large minimum spacing from the contact to adjacent polysilicon;

at the upper level, the contact has nicely sloped sidewalls, so that problems of metal voids and cracking, and electromigration are greatly simplified.

The present application also describes a new method of forming sub-micron contact utilizing Si_3N_4 (or other dielectric film with good etch selectivity to oxide film) as an etch stop for a WET oxide etch. After the wet etch, an anisotropic plasma etch is used to cut a substantially vertical contact hole through the nitride and underlying layers. Thus, the resulting contact hole has a "Y"-shaped profile.

Since the lower silicate glass layer and the nitride layer are not highly planarized, they provide area-efficient protection of the devices from any lateral encroachments which might occur during contact

etching. Most of the planarization is performed in the upper silicate glass layer.

Thus, the lower silicate glass layer and the nitride layer provide self-aligned protection for the gate layer. This protection ensures that no possible combination of geometries will permit the contact etch to create a short circuit to the gate layer.

According to a disclosed class of innovative embodiments, there is provided: A fabrication method, comprising the steps of: providing a partially fabricated integrated circuit structure which includes **transistors**; forming an **interlevel dielectric** structure over said transistors, said interlevel dielectric including at least a **lower layer** having a first composition, a **middle layer** having a second composition which is different from said first composition, and an **upper layer** having a third composition which is different from said second composition; etching through said upper layer, using a relatively isotropic etch process which is selective to said second composition; etching through said middle and lower layers, using a relatively anisotropic etch process, to expose portions of said transistors; and depositing and patterning a thin-film conductor layer, to interconnect said transistors in a desired pattern.

According to another disclosed class of innovative embodiments, there is provided: A fabrication method, comprising the steps of: providing a partially fabricated integrated circuit structure which includes **transistors**; forming an **interlevel dielectric** structure over said transistors, said interlevel dielectric including at least a **lower layer** consisting predominantly of silicate glass, a **middle layer** consisting predominantly of silicon nitride, and an **upper layer**

consisting predominantly of doped silicate glass; etching through said upper layer, using a relatively isotropic etch process which is selective to said second composition; etching through said middle and lower layers, using a relatively anisotropic etch process, to expose portions of said transistors; and depositing and patterning a thin-film conductor layer, to interconnect said transistors in a desired pattern.

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upper layer having a third composition which is different from said second composition; etching through said upper layer, using a wet etch process which is selective to said second composition; etching through said middle and lower layers, using a relatively anisotropic plasma etch process, to expose portions of said transistors; and depositing and patterning a thin-film metal layer, without any intermediate etchback steps, to interconnect said transistors in a desired pattern.

According to another disclosed class of innovative embodiments, there is provided: An integrated circuit, comprising: a **substrate** having **transistors** formed at one surface thereof; an **interlevel dielectric** overlying said transistors, and having at least upper, middle, and lower layers, said middle layer having a different composition from said upper layer and from said lower layer, and having contact holes therein extending vertically therethrough, said contact holes having vertical sidewalls in said lower layer and sloped sidewalls in said upper layer; and a patterned thin-film **metal layer** extending through said contact holes to interconnect said transistors in a desired electrical configuration.

Brief Description of the Drawing

The present invention will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by reference, wherein:

Figure 1 shows a partially fabricated integrated circuit structure, complete through formation of transistor structures;

Figure 2 shows the integrated circuit structure of Figure 1, at a later stage of fabrication according to the present invention;

Figure 3 shows the integrated circuit structure of Figure 2, after masking has been formed and an isotropic etch has been performed at contact hole locations;

Figure 4 shows the integrated circuit structure of Figure 3, after an anisotropic etch has been performed using the contact mask and metal has been deposited and patterned.

Figure 5 is a micrograph which shows an example of a contact fabricated using the disclosed inventions.

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Description of the Preferred Embodiments

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment. However, it should be understood that this class of embodiments provides only a few examples of the many advantageous uses of the innovative teachings herein. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

Figure 1 shows a partially fabricated integrated circuit structure, complete through formation of transistor structures. Fabrication to this point has been entirely conventional, *e.g.* with preparation of silicon wafer **200**, formation of N-wells and P-wells, formation of field oxide **202** to *e.g.* 6000Å, sacrificial oxide grown and stripped, growth of gate oxide **204** to *e.g.* 150Å, threshold voltage adjustment, deposition of polycide gate **210** to *e.g.* 3500Å total thickness, LDD and/or HALO implant or implants, formation of sidewall spacers **220**, and N+ and P+ source/drain implants. This results in the structure of Figure 1.

Thereafter a somewhat unusual interlevel dielectric is deposited. In the presently preferred embodiment, this is performed by the steps of:

1. deposit undoped oxide **230** to *e.g.* 1000 to 2000 Å.
2. deposit a first layer **232** of BPSG (borophosphosilicate glass) or PSG (phosphosilicate glass) to *e.g.* 1000 to 2000 Å.
3. deposit Si_3N_4 layer **234** to *e.g.* 500 to 1000 Å
4. deposit a second layer **236** of BPSG to *e.g.* 3000 to 4000 Å;
5. BPSG reflow/densification (*e.g.* 25 minutes at a temperature of

875°C, in the presently preferred embodiment).

This produces the structure of **Figure 2**. In this structure, note that the reflow of the second BPSG layer has produced some planarization.

A photoresist layer **240** is now deposited, baked, patterned, and developed, to provide apertures over desired contact hole locations. A wet etch is now performed (*e.g.* 250 minutes at a temperature of 25°C in an aqueous solution of 7:1 buffered HF). This etch chemistry has essentially infinite selectivity to nitride, so the nitride layer 234 provides a good etch stop.

This produces the structure shown in **Figure 3**. Note that the wet etch has significantly undercut the photoresist mask 240.

An anisotropic etch is now performed, using *e.g.* a conventional fluoro-etch chemistry which is not selective between oxide and nitride. This cuts through nitride 234, and underlying silicate glass layers 230/232, to expose silicon at the desired contact locations.

Metal **250** is now deposited, *e.g.* 600Å of Ti followed by 1000Å of TiN followed by rapid thermal annealing (to induce silicidation in the contact hole) followed by deposition of a metal such as Al:Cu. The metal layer is then patterned to achieve the desired circuit configuration.

This results in the structure of Figure 4.

Processing may then continue with conventional further steps, *e.g.* deposition of a further interlevel dielectric and a second metal layer (if desired), contact sinter (if needed), deposition and densification of a protective overcoat and removal thereof to expose contact pad locations.

Figure 5 is a micrograph which shows an example of a contact

fabricated using the disclosed inventions.

Advantages

The disclosed innovations provide at least the following advantages:

- metal-to-gate shorts due to overetch during wet oxide etch are completely prevented;
- The full film thickness of the first BPSG film is available for gettering, which improves device reliability. (Silicate glasses, unlike nitride, have the ability to trap ionic impurities.)
- Significant contact aspect ratio reduction to improve metal step coverage, without degrading the contact-to-poly spacing. the reduced aspect ratio provides better sidewall coverage for the adhesion and diffusion-barrier layers which are the first part of the metallization stack, and helps to protect against voids and step coverage difficulties.
- The Si_3N_4 film also provides passivation against hydrogen. Exposure to hydrogen can increase the value of a polysilicon resistor by a factor of 2x or 3x. Thus, in device structures using "poly R" resistor structures, indiffusion of hydrogen may cause a shift in resistor values. The nitride layer thus helps to prevent this, and provides improved stability.
- A simple metallization process, without a plug metal deposition and intermediate etchback, can be used.
- There is no need to reflow the interlevel dielectric after contact etch.

Further Modifications and Variations

It will be recognized by those skilled in the art that the innovative concepts disclosed in the present application can be applied in a wide variety of contexts. Moreover, the preferred implementation can be modified in a tremendous variety of ways. Accordingly, it should be understood that the modifications and variations suggested below and above are merely illustrative. These examples may help to show some of the scope of the inventive concepts, but these examples do not nearly exhaust the full scope of variations in the disclosed novel concepts.

Of course a variety of structures can be used to implement the polysilicon or polycide gate. Similarly, a wide variety of materials, and of combinations of materials, can be used to implement the metal layer.

Of course, the specific etch chemistries, layer compositions, and layer thicknesses given are merely illustrative, and do not by any means delimit the scope of the claimed inventions.

The invention can also be adapted to other combinations of dielectric materials in the interlevel dielectric. For example, phosphosilicate glass or germanosilicate glass can be used instead of the BPSG of the presently preferred embodiment.

The innovative process preferably uses at least a three-level dielectric stack, in which the top layer can be etched selectively with respect to the middle layer. Preferably the top and bottom layers are both silicate glasses, but it will be recognized by those skilled in the art that other materials can be substituted for the silicates or for the nitride. It will also be recognized that additional layers can be added

if desired.

It should be recognized that the first etch step does not have to be perfectly isotropic, but may still function adequately with a modest anisotropy. It should also be noted that the first etch step can be implemented with a high-pressure plasma or afterglow etch instead of a wet etch, IF the etch chemistry used provides high selectivity to nitride.

Similarly, while the sidewall spacers 220 are normally used, they are not strictly necessary to the practice of the invention.

While the disclosed process could be used for via formation, it is much less preferable in that context. The dielectric constant for nitride is about twice that for oxide, so that the parasitic capacitive loading on the metal lines would be increased.

While the inventions have been described with primary reference to a single-poly process, it will be readily recognized that these inventions are equally applicable to double-poly or triple-poly structures and processes. Similarly, while the contact from first metal to first poly and active has been particularly described, it will be readily recognized that the disclosed inventions are equally applicable to processes with multiple layers of metal.

The innovative process teachings may also be adapted for contact formation in bipolar or other device technologies.

Similarly, it will be readily recognized that the described process steps can also be embedded into hybrid process flows, such as BiCMOS or smart-power processes.

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and

varied over a tremendous range of applications, and accordingly the scope of patented subject matter is not limited by any of the specific exemplary teachings given.

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